Electronic Version
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Claims

[c1] What is claimed is:

1. A method of aligning data transmitting timing of a plurality of lanes, the lanes being respectively connected to a plurality of elastic buffers, the method comprising:

determining if an elastic buffer corresponding to the lane adjusts the number of SKP symbols within an ordered set having the COM symbol when a COM symbol is detected on a lane;

resetting a count value corresponding to the lane by a first initial value if said elastic buffer corresponding to the lane adds an SKP symbol to the ordered set having said COM symbol;

resetting said count value corresponding to the lane by a second initial value if said elastic buffer corresponding to the lane deletes said SKP symbol from the ordered set having said COM symbol;

resetting said count value corresponding to the lane by a third initial value if said elastic buffer corresponding to the lane does not adjust the number of SKP symbols within the ordered set having said COM symbol;

increasing said count value corresponding to the lane by an increment value when a COM symbol is not detected

on the lane; and

aligning said data transmitting timing of the lanes according to a plurality of count values respectively corresponding to the lanes if a COM symbol is not detected on the lanes within a predetermined period of time.

[c2] 2. The method of claim 1, wherein said second initial value is greater than said third initial value and said third initial value is greater than said first initial value.

[c3] 3. The method of claim 1, wherein a difference between said second and said third initial values is equal to a difference between said third and said first initial values.

[c4] 4. The method of claim 1, wherein each of a difference between said second said and third initial values and a difference between said third and said first initial values is equal to said increment value.

[c5] 5. The method of claim 1, further comprising: recording an offset value, wherein said offset value is the minimum value among said count values.

[c6] 6. The method of claim 5, further comprising: when said COM symbol is detected on the lane, resetting said offset value by said second initial value to if said elastic buffer corresponding to the lane deletes said SKP symbol from the ordered set having said COM symbol.

[c7] 7. The method of claim 5, further comprising:
when said COM symbol is detected on the lane, resetting said offset value by the third initial value if said elastic buffer corresponding to the lane deletes said SKP symbol from the ordered set having said COM symbol and said offset value currently corresponds to said first initial value.

[c8] 8. The method of claim 5, further comprising:
when said COM symbol is detected on the lane, resetting said offset value by said first initial value if said elastic buffer corresponding to the lane adds said SKP symbol to the ordered set having said COM symbol.

[c9] 9. The method of claim 5, further comprising:
when said COM symbol is detected on the lane, resetting said offset value by said third initial value if said elastic buffer corresponding to the lane does not adjust said number of SKP symbols within the ordered set having said COM symbol.

[c10] 10. The method of claim 5, further comprising:
when said COM symbol is not detected on the lane, increasing said offset value by said increment value.

[c11] 11. The method of claim 5, further comprising:
calculating a plurality of differences between said count

values and said offset value, and aligning the data transmitting timing of the lanes according to said differences.

[c12] 12. The method of claim 1, further comprising:
if said COM symbol is detected on lanes, triggering a control signal having a transition from a first logic level to a second logic level; and
if said COM symbol is not detected on lanes, resetting said control signal wherein said control signal has a transition from the second logic level to the first logic level.

[c13] 13. The method of claim 12, wherein said data transmitting timing of the lanes is aligned if a period when said control signal holds the first logic level is longer than the predetermined period of time.

[c14] 14. A timing alignment circuit for aligning data transmitting timing of a plurality of lanes, the lanes respectively connected to a plurality of elastic buffers, said timing alignment circuit comprising:
a plurality of detectors coupled to the lanes for detecting COM symbols within ordered sets transmitted via the lanes;
a plurality of first counters for counting a plurality of count values corresponding to the lanes;
a decision logic coupled to said detectors and said first

counters for determining whether an elastic buffer corresponding to a lane adjusts the number of SKP symbols within an ordered set having said COM symbol when said COM symbol is detected on the lane, wherein said decision logic resets a count value corresponding to the lane by a first initial value if said elastic buffer corresponding to the lane adds an SKP symbol to the ordered set having said COM symbol, the decision logic resets said count value corresponding to the lane by a second initial value if said elastic buffer corresponding to the lane deletes said SKP symbol from the ordered set having said COM symbol, and said decision logic resets said count value corresponding to the lane by a third initial value if said elastic buffer corresponding to the lane does not adjust the number of SKP symbols within the ordered set having said COM symbol;

a plurality of de-skew buffers; and

a controller coupled to said first counters and said de-skew buffers for driving said de-skew buffers to align the data transmitting timing of the lanes according to said count values respectively corresponding to the lanes if said detectors do not detect said COM symbol within a predetermined period of time;

wherein if said detector does not detect said COM symbol on the lane, a first counter corresponding to the lane increases said count value corresponding to the lane by

an increment value.

[c15] 15. The timing alignment circuit of claim 14, wherein said second initial value is greater than said third initial value and said third initial value is greater than said first initial value.

[c16] 16. The timing alignment circuit of claim 14, wherein a difference between said second and said third initial values is equal to a difference between said third and said first initial values.

[c17] 17. The timing alignment circuit of claim 14, wherein each of a difference between said second and said third initial values and a difference between said third and said first initial values is equal to said increment value.

[c18] 18. The timing alignment circuit of claim 14, further comprising:
a second counter coupled to said decision logic for counting an offset value, wherein said offset value is the minimum value among said count values.

[c19] 19. The timing alignment circuit of claim 18, wherein when said COM symbol is detected on the lane, said decision logic determines if said elastic buffer corresponding to the lane adjusts the number of SKP symbols within the ordered set having said COM symbol for resetting

said offset value by one of said first, said second, and said third initial values.

[c20] 20. The timing alignment circuit of claim 18, wherein if said detectors do not detect said COM symbol on the lanes, said second counter increases said offset value by said increment value.

[c21] 21. The timing alignment circuit of claim 14, wherein said controller calculates a plurality of differences between said count values and said offset value, and aligns the data transmitting timing of the lanes according to said differences.

[c22] 22. The timing alignment circuit of claim 14, further comprising:
a trigger coupled to said detectors and said controller for generating a control signal used for controlling said controller to drive said de-skew buffers to align the data transmitting timing of the lanes;
wherein if said detectors detect said COM symbol on the lanes, said trigger triggers said control signal having a transition from a first logic level to a second logic level, and if said detectors do not detect said COM symbol on the lanes, said trigger resets said control signal wherein said control signal has a transition from the second logic level to the first logic level.

[c23] 23. The timing alignment circuit of claim 22, wherein said controller aligns the data transmitting timing of the lanes if a period when said control signal holds the first logic level is longer than the predetermined period of time.

[c24] 24. A method of aligning data transmitting timing of a plurality of lanes comprising:
transmitting a plurality of test data sets on each lane; and
aligning the data transmitting timing of each lane according to a transmitting status of a test data set on each lane.

[c25] 25. The method of claim 24, wherein each of the test data sets comprises a plurality of COM symbols and a plurality of SKP symbols.

[c26] 26. The method of claim 25, wherein the data transmitting timing of each lane is aligned according to the number of the COM symbols and the number of the SKP symbols within each lane.

[c27] 27. The method of claim 25, further comprising:
when the last COM symbol within the test data sets is detected, aligning the data transmitting timing of each lane by the number of the COM symbols and the number

of the SKP symbols.

[c28] 28. The method of claim 24, further comprising:
determining an offset value of each lane according to the test data sets; and
aligning the data transmitting timing of each lane by said offset value.

[c29] 29. The method of claim 24, further comprising:
determining an offset value of each lane according to the test data sets; and
determining the amount of delay applied to each lane by said offset value.